IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Ward D. Parkinson et al.	§	Art Unit:	2827
Serial No.:	10/634,153	§	Examiner:	Viet Q. Nguyen
Filed:	August 4, 2003	§		
For:	Analog Phase Change Memory	§	Atty Docket:	ITO.0553US (P16341)

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APPEAL BRIEF

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Date of Deposit: December 1, 2005
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Cynthia L. Hayden

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-25 (Rejected).

Claims 1-25 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

No amendments have been made. A Notice of Appeal was filed in response to the final Office action.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. A method comprising:

forming an analog memory (50, Figure 2, specification at page 4, lines 12-23) using a phase change material (42, Figure 2, specification at page 4, lines 12-23).

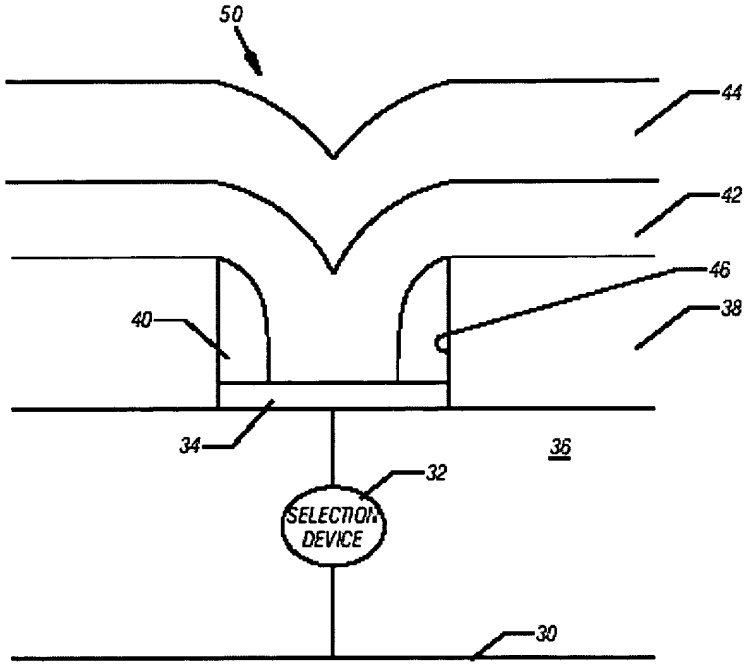

FIG. 2

11. A memory comprising:

a phase change material (42, Figure 2, specification at page 4, lines 12-23); and

a circuit (22, Figure 1, specification at page 3, lines 15-20) to write analog data using said phase change material.

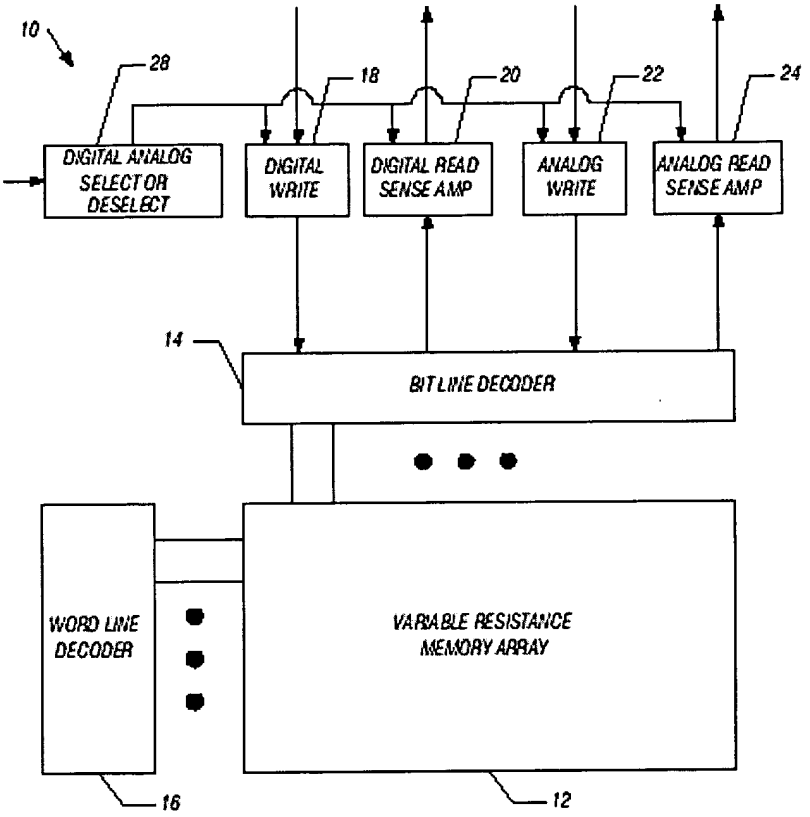

FIG. 1

21. A system comprising:

a processor (510, Figure 3, specification at page 10, lines 22-24);

a wireless interface (540, Figure 3, specification at page 10, lines 16-21) coupled to said processor; and

a semiconductor memory (530, Figure 3, specification at page 4, lines 12-23) coupled to said processor, said memory including a phase change material (412, Figure 2, specification at page 4, lines 12-23) and a circuit (22, Figure 1, specification at page 3, lines 15-20) to write analog data for storage using said phase change material.

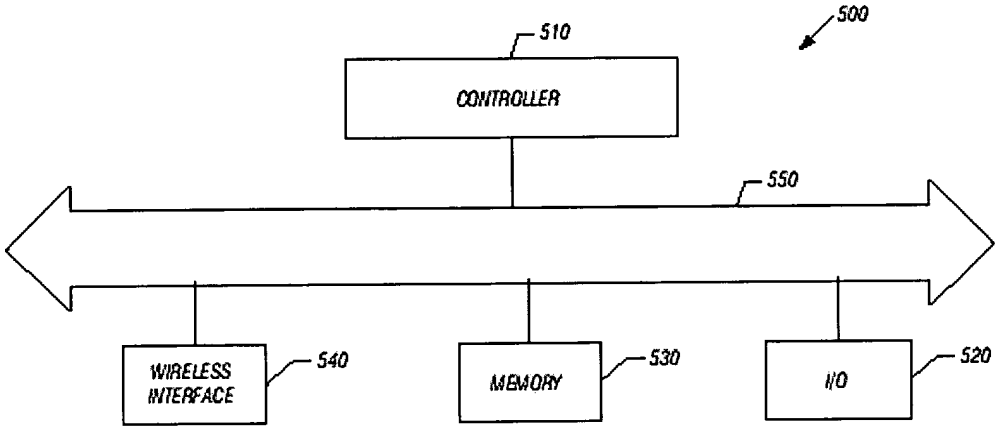

FIG. 3

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. **Are Claims 1-25 Unpatentable Over Ovshinsky?**

B. **Are Claims 1-25 Unpatentable Over Klersy?**

C. **Are Claims 1-25 Unpatentable Over Czubatyj '046?**

D. **Are Claims 1-25 Unpatentable Over Van Brocklin?**

E. **Are Claims 1-25 Unpatentable Over Czubatyj '340?**

ARGUMENT

A. Are Claims 1-25 Unpatentable Over Ovshinsky?

All of the claims are rejected under Section 103 over any one of Ovshinsky, Klersy, Czubatyj, Van Brocklin, or Czubatyj '340 or '046.

However, every one of these references relates to a digital system and not one of them relates to an analog system.

More particularly, each of them store states, not analog signals. States, regardless of the number of states, is commensurate with digital storage. There is no storage of states in analog storage.

With respect to Ovshinsky, it is pointed out that in the background prior art there is a discussion of an ovonic EEPROM that is capable of both analog and digital forms of information storage. However, the material pointed out by the Examiner indicates that what is referred to here is not storage of the analog signal itself, but storage of a representation, in digital form, of the analog signal. In other words, the analog signal is converted into gray scales or other digital representations and stored.

This is explicitly explained in column 1, lines 57-60, where there is a discussion of gray scale values. Gray scale is the digitization of the analog information. See the attachment to the previous response. This is further substantiated by the material at column 20, lines 56 *et. seq.*, talking about the dynamic range of resistance allows for broad "gray scale and multilevel analog memory storage." Thus, levels in gray scale teach digital storage of digitized analog information. Similarly, in column 20, line 61, it is explained that it is binary information that is stored in the cell. Further, multilevel storage, which preceded analog memory storage in line 57, is explained to be binary information in pseudo-analog form. Instead, analog levels are used and provided with the capability of storing n bits of binary information. There can be no doubt that analog information is converted to digital form (digitized) and this is what is being stored. While this is called analog storage, apparently because an analog signal is digitized and stored, it does not amount to storing an analog value as an analog value in the storage. While the reference's terminology is awkward and perhaps incorrect, the intent is clear.

B. Are Claims 1-25 Unpatentable Over Klersy?

The Klersy patent appears to have the same information as the Ovshinsky patent and the same comments apply.

C. Are Claims 1-25 Unpatentable Over Czubatyj '046?

The Czubatyj '046 patent appears to have the same information and the same comments apply.

D. Are Claims 1-25 Unpatentable Over Van Brocklin?

The Van Brocklin patent also stores states. This is explicitly conceded in the second through the fourth line of page 6 of the office action and is clearly set forth in the Van Brocklin reference. If an analog signal is being stored there would be no states, be they multiple states or otherwise. Thus, in analog storage, level states are not stored, an analog signal is stored. The discussion of levels and states makes it absolutely clear that Van Brocklin is storing digitized representations of analog information.

For example, in column 5, lines 26-37, it is explained that for a given program state, there is a sensed current. There would not be states if analog storage was involved. Further, there is a discussion of four possible states and the note that any number of states could be implemented. In analog storage there would be no states. Clearly, the discussion is of digital storage. Similarly, with respect to the sense circuitry at column 5, lines 55-61, there is discussion of the detection of a particular value of an electrical parameter, plainly, a discussion of a digital storage device. Also, at column 5, lines 62-63, there is discussion of a memory cell that has one state-change device that can be programmed to multiple states.

Similarly, in connection with Figure 8, and column 9, lines 38 *et. seq.*, there is a discussion of states and programming to discrete states. Therefore, there can be no dispute that the information described in this reference involves digital storage. See, for example, claim 1 calling for a state change device, claim 11 calling for a state change device having at least three states, claim 21 calling for a state change device, and claim 31 calling for a state change device.

E. Are Claims 1-25 Unpatentable Over Czubatyj '340?

The Czubatyj '340 patent suffers from the same deficiencies described above. The fact that at column 2, lines 25-35, there is discussion of electrically detectable forms does not militate against determining states. The only alternatives described in column 2, lines 30-35, is what is called a binary value, a logical one or a logical zero, or an analog value such as a gray scale

value or other electrically detectable form. As pointed out before, and as explained in the attachment to the previous response, a gray scale value is a digitized analog form. Clearly, the reference teaches what might be loosely and incorrectly called storing analog information, but doing so by digitizing that information. As such, the reference fails to meet the claim limitations.

Specifically, claim 1 calls for forming an analog memory using a phase change material. Claim 2 calls for selectively enabling digital or analog storage. None of the references enable selective digital or analog data to be stored, not only because they never store analog data in analog form, but because they do not allow such selectivity.

The Applicants' usage of analog non-volatile memory is consistent with that set forth in U.S. Patent 5,745,409 at column 1, lines 26-39 cited by Applicants. (See Evidence Appendix). This demonstrates that those skilled in the art understand that analog non-volatile memories are distinct from digital non-volatile memories and that they store analog, not digital, representations of analog information.

Applicants respectfully request that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: December 1, 2005

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CLAIMS APPENDIX

The claims on appeal are:

1. A method comprising:
forming an analog memory using a phase change material.

2. The method of claim 1 including selectively enabling either digital or analog data to be stored in said memory.

3. The method of claim 1 including forming a phase change material having a programmably variable resistance for a plurality of cells.

4. The method of claim 3 including enabling said cells to be addressably located along rows and columns.

5. The method of claim 1 including forming a phase change material in a pore.

6. The method of claim 5 including forming a selection device to enable the control of current through said phase change material.

7. The method of claim 1 including enabling said memory to store in a single cell one of at least three different resistance values.

8. The method of claim 7 including enabling the resistance of the cell to be set by varying the magnitude of a programming current to the cell.

9. The method of claim 8 including enabling the resistance of the cell to read and readjust using a different programming current.

10. The method of claim 9 including enabling a resistance to be set in said cell proportional to a voltage or current characteristic to be stored.

11. A memory comprising:
a phase change material; and
a circuit to write analog data using said phase change material.

12. The memory of claim 11 including a circuit to selectively enable either digital or analog data to be stored in said memory.

13. The memory of claim 11 wherein said phase change material has a programmably variable resistance.

14. The memory of claim 13, said memory to store digital and analog data.

15. The memory of claim 14 wherein said memory to selectively store digital or analog data.

16. The memory of claim 15 including a circuit to enable a user to select analog or digital data storage.

17. The memory of claim 16 including an analog read sense amplifier, a digital read sense amplifier, an analog write circuit, and a digital write circuit.

18. The memory of claim 11 including a substrate, an insulator formed over said substrate, a pore defined in said insulator, and a phase change material in said pore.

19. The memory of claim 11 including a plurality of cells including a phase change material, said memory including a plurality of conductive lines to selectively enable access to said cells.

20. The memory of claim 19 wherein said phase change material includes a chalcogenide.

21. A system comprising:

a processor;

a wireless interface coupled to said processor; and

a semiconductor memory coupled to said processor, said memory including a phase change material and a circuit to write analog data for storage using said phase change material.

22. The memory of claim 21 including a circuit to selectively enable either digital or analog data to be stored in said memory.

23. The system of claim 21, said memory to store digital and analog data.

24. The system of claim 23 wherein said memory to selectively store digital or analog data.

25. The system of claim 24 including a circuit to enable a user to select analog or digital data storage.

EVIDENCE APPENDIX

RELATED PROCEEDINGS APPENDIX

None

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
ITO.0553US

In Re Application Of: **Ward D. Parkinson et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/634,153	August 4, 2003	Viet Q. Nguyen	21906	2827	5107

Invention: **Analog Phase Change Memory**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **October 18, 2005**

The fee for filing this Appeal Brief is: **$500.00**

☒ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**

☐ Payment by credit card. Form PTO-2038 is attached.

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Signature

Dated: **December 1, 2005**

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December 1, 2005
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Signature of Person Mailing Correspondence

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